REMARKS

In the Office Action of May 20, 2004, claims 1-44 were presented for examination and of these, claims 1-44 were rejected. In response, Applicant requests reconsideration and amends claims 1, 8, 13, 16, 18, 22, 28, 30, 33, 36-39 and 40. Claims 7 and 21 are cancelled without prejudice or disclaimer. No new claims have been added.

Specification

The Office indicates that the title of the invention is not descriptive, and requires a new title. According, the title is amended above to "Method and apparatus for interconnecting analog and digital sections of A/D and D/A converters." If the Examiner does not find this title suitably descriptive, perhaps he can suggest one.

Claim Rejections- 35 USC 102

The Office Action rejects Claims 1-3, 5-6 and 39 as anticipated by Lipasti. In addition, Claims 18, 20 and 40 are rejected as anticipated by Melanson.

Lipasti

Claim 1 has been amended to incorporate the features of claim 7. Claim 7 was not rejected over Lipasti. Accordingly, amended claim 1 is allowable over Lipasti and the rejection of claims 1-3 and 5-6 is now moot and should be withdrawn.

Likewise, claim 39 has been amended to have method scope similar to that of apparatus claim 1 and more particularly to recited "receiving the n-bit digital output signal across said interface and processing the received n-bit signal to generate an output digital signal." Such limitation, which correlates with the subject matter of claim 7 which made it allowable over Lipasti, likewise makes claim 39 allowable. The rejection should accordingly be withdrawn.

Claim 39 has also been amended, as have other method claims, to replace the word "steps" with "acts" in an effort to make it clear that Applicant seeks to avoid the narrow construction of the sixth paragraph of §112.

Melanson

Claims 18, 20 and 40 were rejected as anticipated by Melanson. Claim 18 has been amended to include the limitations of claim 21, which was not similarly rejected. Accordingly, claim 18 is now allowable without further comment. Claim 21 is cancelled, as redundant. Claim 20 depends from claim 18 so it is similarly allowable. The dependencies of claims 22, 28, 30 and 33 are conformed. Claim 40 has been amended to recite the features of claim 18, though in method form. Specifically, amended claim 40 now calls for "processing the digital input signal to generate said s-bit digital signal and to deliver said s-bit signal to said interface." Melanson does not disclose this limitation, which is why claim 21 was not rejected as anticipated. Accordingly, amended claim 40 is not anticipated.

Thus, the rejection of claims 18, 20 and 40 as anticipated by Melanson should be withdrawn.

Please note that claim 40 has also been amended to change "steps" to "acts" for the same reason given above.

Claim Rejections – 35 U.S.C. §103

Three rejections have been set fourth under 35 U.S.C. §103(a). All are based on Lipasti as a primary reference in view of Melanson as a secondary reference and, in some cases, further in view of a tertiary reference (either Desrosiers et al. or Tang et al.) Manifestly, these rejections are all flawed and unsupportable, as demonstrated below.

We should first turn our attention to the subject invention and then address the references and rejections.

Reconsideration is requested.

As explained in the specification, the present invention is concerned with providing an improved circuit and method for interconnecting the analog and digital sections of analog-to-digital and digital-to-analog converters, which overcomes a number of problems associated with prior art techniques. One prior art approach to this problem is to serialize the data transfer between the analog and digital sections. This requires the conversion of the data from parallel to serial format prior to outputting across the interface. However this technique necessitates the use of a high frequency clock, which is often difficult to supply. Even when such a high

frequency clock is available, its use can often impact negatively on the performance of the circuit, due to increased signal interference.

An alternative prior art approach used to interconnect analog and digital sections involves transferring data using a parallel interface. This has the significant drawback of increasing the device pin count, as a parallel data bus requires a separate pin per data bit.

In one aspect, the present invention overcomes the problems associated with the prior art by providing a signal processing apparatus for converting between the analog and digital domains comprising a first section and a second section which are connectable to one another by an interface. The first section comprises a means for converting an input signal into a multi-bit digital format and an input converter for quantizing the multi-bit signal so as to generate a lower resolution digital signal which can be sent across the interface. The second section comprises a processor which receives the lower resolution signal and to processes the received signal to generate an output digital signal.

Lipasti, by contrast, is concerned with controlling the level of a pulse-density-modulated (PDM) signal generated by a sigma-delta modulator. The document discloses an A/D converter which converts an analog input signal into a 1-bit PDM format by a first sigma delta modulator. Level control is then performed by multiplying the single PDM signal by a multi-bit multiplier in order to obtain a multi-bit number stream. It is then reconverted into a single-bit PDM signal by means of a second digital sigma delta modulator.

The purpose of the circuit of Lipasti is to enable the amplification of a PDM signal without a significant increase in noise level. This development may be very useful in particular applications, for example in the area of audio applications, and in filtering circuits.

Melanson, on the other hand, discloses an improved digital to analog conversion circuit for use with 1-bit audio data, such as that provided on a CD, or a DAT or a DVD player. The circuit includes a digital-to-analog converter which uses a single-bit sigma delta modulator and a multiple-bit digital-to-analog converter. The motivation behind Melanson is to provide an improved circuit suitable for integration with the Sony/Philips 1-bit recording systems with a low signal-to-noise ratio.

The Examiner appears to reason that the circuit of the present invention is obvious due to the number of circuit components which are common between the circuits of Melanson and

Lipasti and the claimed invention. This analysis is fundamentally flawed. It ignores the details of how and why those components are put together in a unique way, and the absence of motivation to do so.

Neither Lipasti nor Melanson is concerned with one of the problems addressed by the present invention, which is to provide an improved method for interconnecting separate analog and digital sections of analog-to-digital and digital-to-analog converters suitable for use in any application where such data transfer is required. In contrast, both Lipasti and Melanson are purely related to providing an improved circuit for use in an application-specific environment. Furthermore, neither prior inventor had to contend with interface issues similar to the issues addressed by the claimed invention, i.e. how to transfer data from an analog to a digital section (and vice versa) without signal degradation and without increasing the pin count.

Further, it would not have been obvious for a person of ordinary skill, when confronted with that problem, to combine the teachings of Lipasti and Melanson, which are purely concerned with reducing noise in audio environments. Neither was there a motivation to combine the references for another purpose, serendipitously yielding the claimed invention. Only hindsight guided by Applicant's disclosure could lead to such a combination. This is pure, prohibited "Monday-morning quarterbacking."

Moreover, even if the skilled person had been motivated to combine the two teachings, it would have required considerable additional inventive input to start from the teachings of these documents, with circuits tailored to provide an application-specific output, and to modify these circuits so that they could be combined in such a manner as to result in the claimed apparatus, article and method of the present invention.

For the foregoing reasons and the reasons discussed above relative to the anticipation rejection, all of the independent claims of the present invention are allowable over Lipasti and Melanson, taken singly, together or combined with the tertiary references. Consequently, their dependent claims also are allowable.

Miscellaneous

Some amendments made herein are not responsive to any objection or rejection, and are solely for improved form.

Claims 8, 18, 22, 36 and 37 are amended to remove redundancy when comparing bit resolutions.

Claims 36 and 37 are amended in form to remove any ambiguity as to whether the references to claims 1 and 18, respectively, were intended to be limiting. A conforming amendment is made to claim 38.

Conclusion

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 20, 2004.

Nicole Millette Hawes

Respectfully submitted,

Paschal T. Minogue, Applicant

By:

Steven J. Henry, Reg. No. 27,900
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 646-8000

Attorney Docket No.: T0461.70042US00
X09/20/04